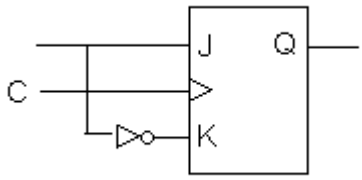
Study Questions and Answers

Combinatorial and Sequential Logic

1. Show that a JK flip flop can be converted to a D flip flop with an inverter between the J and K inputs



2. Design a combinational circuit with three inputs x, y, z and three outputs A, B, C . When the binary input is 0, 1, 2, 3 the binary output is one greater than the input. When the binary input is 4,5,6, or 7 the binary output is one less than the input.

x	y	z	A	B	C
0	0	0	0	0	1
0	0	1	0	1	0
0	1	0	0	1	1
0	1	1	1	0	0
1	0	0	0	1	1
1	0	1	1	0	0
1	1	0	1	0	1
1	1	1	1	1	0

$A = yz + xz + xy$
$B = x \oplus y \oplus z$
$C = z'$

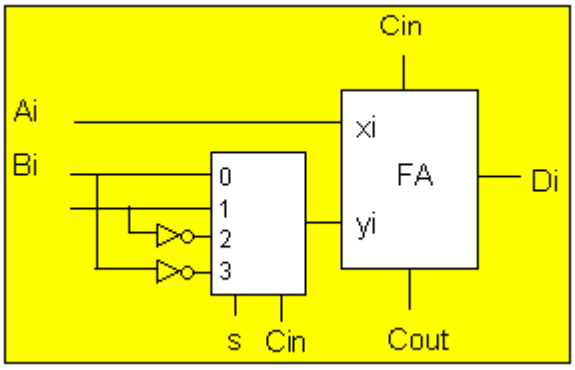
3. Design a counter with JK flip flops that counts 1,3,5,7, 1,3,5,…

A	B	C	JA	KA	JB	KB	JC	KC
0	0	1	0	X	1	X	X	0
0	1	1	1	X	X	1	X	0
1	0	1	X	0	1	X	X	0
1	1	1	X	1	X	1	X	0
0	0	1	0	X	1	X	X	0

$JA = B$ $KA = B$
$JB = 1$ $KB = 1$
$JC = KC = 0$

4. Design an arithmetic circuit with one selection variable s and two n-bit data inputs A and B. The circuit generates the following four arithmetic operations in conjunction with the input carry Cin. Draw the logic diagram for the first two stages.

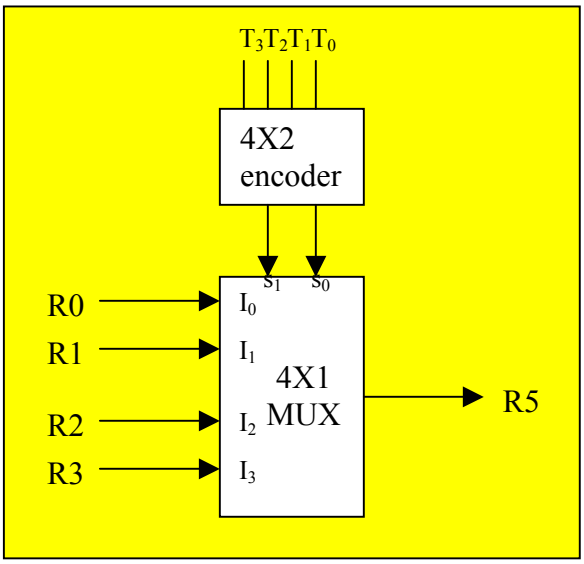
S	Cin = 0	Cin = 1
0	D = A + B (add)	D = A + 1 (increment)
1	D = A – 1 (decrement)	D = A + B' + 1 (subtract)



5. The outputs of four registers, R0, R1, R2, and R3 are connected through 4-to-1 line multiplexers to the inputs of a fifth register, R5. Each register is 8 bits long. The required transfers are dictated by four timing variables T_0 through T_3 as follows:

   T_0 : R5 ← R0
   T_1 : R5 ← R1
   T_2 : R5 ← R2
   T_3 : R5 ← R0

   The timing variables are mutually exclusive, which means that only one variable is equal to 1 at any given time, while the other three are equal to 0. Draw a block diagram showing the hardware implementation of the register transfers. Include the connections necessary from the four timing variables to the selection inputs of the multiplexers and to the load input of R5.



6. A digital computer has a common bus system for 16 registers of 32 bits each. The bus is constructed with multiplexers.
    a. How many selection inputs are there in each multiplexer?
    b. What size of multiplexers are needed?
    c. How many multiplexers are there in the bus?

7. The operations to be performed with a flip flop are specified as follows:

    x T_3 : $F \leftarrow 1$ Set F to 1
    y T_1 : $F \leftarrow 0$ Clear F to 0
    z T_2 : $F \leftarrow F'$ Complement F
    w T_5 : $F \leftarrow G$ Transfer value of G to F

    Otherwise the content of F must not change. Draw the logic diagram showing the connections of the gates that form the control functions and the inputs of flip flop F. Use a JK flip flop.